ADSL / VDSL Line Simulation

A Feasibility Study and Initial Design

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Abstract

This dissertation describes an MSc project to investigate the feasibility of building a digital hardware line simulator for use as ADSL and VDSL test environments during modem development. The simulation requirement interms of crosstalk, noise and the physical line effects of twisted copper access pairs at DSL frequencies are determined. A simulation model using both time and frequency domains is brought forward with suitable DFT parameters calculated. Modelling of the physical line's attenuation and phase shift through frequency domain filtering is developed. Two practical ADSL line simulator implementation paths using DSP and FPGA devices are evaluated according to five performance and development metrics. Initial high level and revised logic level designs are undertaken using Xilinx FPGAs and FFT modules. Functionality is tested and performance evaluated using Xilinx Foundation software. Finally, future adaptability to VDSL line simulation is discussed. 44 references included.