Preface

The aim of this MSc project was to investigate the possibility of constructing a compact PC controlled hardware line simulator suitable for replacing the traditional twisted copper pair access cable as a test environment for ADSL and VDSL modems under design. The dissertation covers a wide range of subjects, ranging from investigation of the copper pair at DSL transmission frequencies, through to an in depth low-level initial design based on Xilinx FPGAs.

The main areas of the dissertation cover:

- The behaviour of the twisted copper pair at DSL frequencies in chapters 2 and 3.
- Simulation requirements and suitable signal processing methods in chapters 4 and 5.
- ANSL DMT ADSL signal modelling using Matlab in chapter 6.
- High level designs for ADSL simulators comparing DSP and FPGA solutions in chapter 7.
- A revised high level design using FPGA processing blocks in chapter 8.
- In depth low-level logic circuitry and functionality testing of the revised design using the latest Xilinx FPGAs in chapter 9.
- Possible extension to VDSL line simulation in chapter 10.

The low-level logic designs in chapter 9 assume the reader is conversant in designing Xilinx FPGAs using the Foundation design environment and includes complex logic designs without step by step explanation of their operation which is secondary to the aim of the project and dissertation. Included on the CD ROM are all Foundation schematic, simulation and waveform files associated with all the circuits of chapter 9.

In addition to the project design files for use in the Xilinx Foundation environment, the CD ROM also includes full data sheets in PDF format of all devices mentioned, as well as pertinent DSL tutorials from various sources and the latest Xilinx Foundation upgrade files necessary for the design. In order to compile and run simulations on the project designs, a minimum of 128 Mbytes of RAM is required, otherwise excessive hard disk activity occurs with the associated extended processing times.

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